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Keynote

Massive Parallelism in Intel's Graphics Processors

Tomas Akenine Möller

Abstract
The performance improvement in graphics processors over the past decade has been tremendous, and it is intriguing to see that the graphics part of the chip die now is larger than for the CPU part. In this presentation, I will explain how this kind of parallelism can be achieved by describing the graphics processor in Intel's Broadwell architecture. In addition, I will show how a ray tracer can be mapped, using OpenCL, to such an architecture with shared memory, and will demonstrate interactive performance.

Short Biography
Tomas Akenine Möller is a professor in computer science with specialization in computer graphics and image processing at the Department of Computer Science, Lund University, Sweden. Over the past years, he has built the computer graphics group, LUGG (Lund University Graphics Group), there. He received an MSc in Computer Science and Engineering from Lund in 1995, and went on to Chalmers University of Technology, where he got his PhD in computer graphics in 1998. During 2000, he was a post doc at UC Berkeley, and also spent some time at UC San Diego (2004/2005) as a visiting researcher. Tomas has been co-papers-chairing Graphics Hardware (2004), Eurographics Symposium on Rendering (2006), and Eurographics 2010. He currently works part time at Intel in Lund as a tech lead with a fantastic team of graphics researchers. In December 2008, Intel acquired Swiftfoot Graphics, which is a company he co-founded with three of his PhD students. Tomas is also a co-author of the book Real-Time Rendering. He has written 80+ papers, and still counting.

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